ISL6142/52 EVAL1 Board

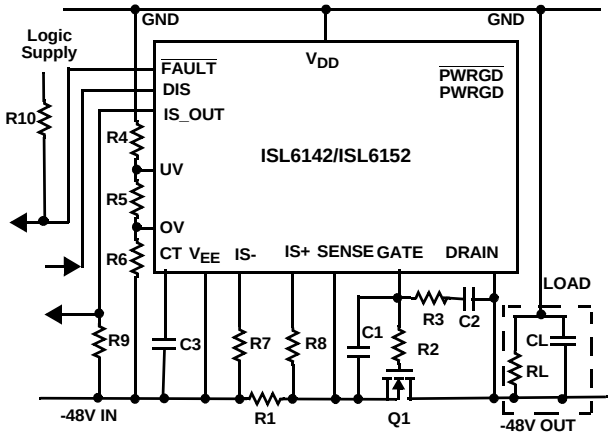
Negative Voltage Hot Plug Controller

The ISL6142/52 are 14 pin, negative voltage hot plug controllers that allow a board to be safely inserted and removed from a live backplane. Inrush current is limited to a programmable value by controlling the gate voltage of an external N-channel pass transistor. The pass transistor is turned off if the input voltage is less than the Under-Voltage threshold, or greater than the Over-Voltage threshold. The $\overline{PWRGD}$/PWRGD outputs can be used to directly enable a power module. When the GATE and DRAIN voltages are both considered good the output is latched in the active state.

The IntelliTrip™ electronic circuit breaker and programmable current limit features protect the system against short circuits. When the Over-Current threshold is exceeded, the output current is limited for a time-out period before the circuit breaker trips and shuts down the FET. The time-out period is programmable with an external capacitor connected to the CT pin. If the fault disappears before the programmed time-out, normal operation resumes. In addition, the IntelliTrip™ electronic circuit breaker has a fast Hard Fault shutdown, with a threshold set at 4 times the Over-Current trip point. When activated, the GATE is immediately turned off and then slowly turned back on for a single retry.

The IS+, IS-, and IS_{OUT} pins combine to provide a load current monitor feature that presents a scaled version of the load current at the IS_{OUT} pin. Current to voltage conversion is accomplished by placing a resistor (R9) from IS_{OUT} to $-V_{IN}$

Typical Application



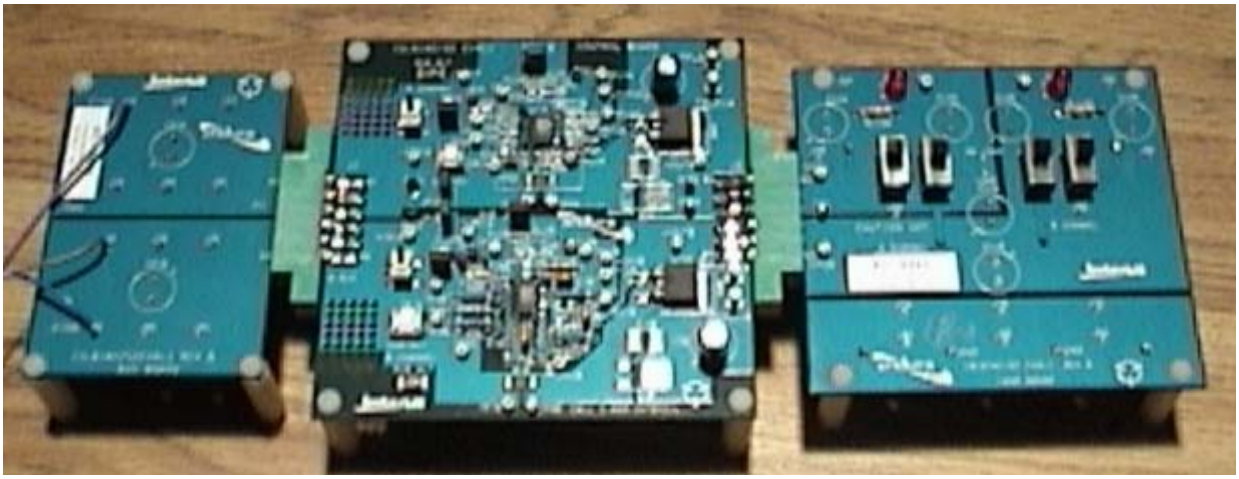
R1 = 0.02Ω (1%)
R2 = 10Ω (5%)
R3 = 18KΩ (5%)
R4 = 549KΩ (1%)
R5 = 6.49KΩ (1%)
R6 = 10KΩ (1%)
R7/R8 = 400Ω (1%)
R9 = 4.99KΩ (1%)
R10 = 5.1KΩ (10%)
C1 = 150nF (25V)
C2 = 3.3nF (100V)
C3 = 1500pF (16V)
Q1 = IRF530
CL = 100µF (100V)
RL = Equivalent load resistance

Features

- Operates from -20V to -80V (-100V Absolute Max Rating)
- Programmable Inrush Current
- Programmable Time-Out
- Programmable Current Limit
- Programmable Over-Voltage Protection
- Programmable Under-Voltage Protection
  - 135 mV of hysteresis ~4.7V of hysteresis at the power supply
- V_{DD} Under-Voltage Lock-Out (UVLO) ~ 16.5V
- IntelliTrip™ Electronic Circuit Breaker distinguishes between severe and moderate faults
  - Fast shutdown for short circuit faults with a single retry (fault current > 4X current limit value)
- $\overline{FAULT}$ output reports the occurrence of an Over-Current Time-Out
- Disable input controls GATE shutdown and resets Over-Current fault latch
- Current Monitor Function
  - IS_{OUT} provides a scaled version of the load current
  - A resistor from IS_{OUT} to $-V_{IN}$ provides current to voltage conversion
- Power Good Control Output
  - Output latched “good” when DRAIN and GATE voltage thresholds are met
  - ($\overline{PWRGD}$ active low: ISL6142 (L version)
  - PWRGD active high: ISL6152 (H version)

Applications

- VoIP (Voice over Internet Protocol) Servers
- Telecom systems at -48V
- Negative Power Supply Control
- +24V Wireless Base Station Power



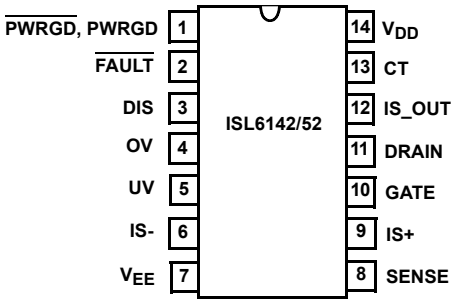
BUS BOARD CONTROL BOARD LOAD BOARD

FIGURE 1. THREE BOARD SET PHOTOGRAPH

Related Literature

- ISL6142/52 Hot Plug Controller, Document # FN9086
- ISL6141/51 Hot Plug Controller, Document # FN9079
- ISL6140/50 Hot Plug Controller, Document # FN9039
- ISL6140/50 EVAL1 Board Set Document # AN9967
- ISL6140/41 EVAL1 Board Set Document # AN1020
- ISL6116 Hot Plug Controller, Document # FN4778

Pinout



NOTE: See www.intersil.com/hotplug for more information. Fully populated; requires only 48V and 5Vpower supplies to exercise all IC functions

ISL6142/52 Evaluation Board Overview

This document assumes the reader is familiar with the hot plug concept, and has a copy of the ISL6142/52 data sheet (FN9086)

The ISL6142/52 EVAL1 Board Set is made up of 3 boards to simulate live plug-ins (see Figures 1, 2, and 5 for various representations):

- BUS board: Input -48V power bus
- CONTROL board: IC hot-plug functions
- LOAD board: Load resistors and capacitors
- Two independent channels for comparison measurements
- Channel B configured with socketed through-hole components to facilitate device analysis

This evaluation platform allows the user to simulate plugging a board into a live edge connector or simulate plugging a live load into a motherboard.

- Most component values have been optimized for performance at -48V and some components will need to be changed to evaluate the device at the extremes of the operating voltage range. For example, the OV threshold is set to 56V to safely manage the temperature of the load board and accommodate the power dissipation rating of the load resistors. The Over-Current threshold is set to 185mA with a 0.270Ω sense resistor (R1) for the same reason. The lower threshold also allows the evaluation of the current limit and hard fault response with more standard/available supplies. Note that the board is capable of operating at much higher voltages (-80V), and currents (17A) with the appropriate application components. When evaluating the device at lower voltages, the user should keep in mind that the UV (turn on) threshold is set at -44.5 volts. The device will shut down the FET when the supply falls below 39.7V (135mV hysteresis). Also, the brightness of the power good LED fault indicators (D5A/B) is determined by the supply voltage through a current limiting resistor. Operating the

device at lower supply levels will produce a lower intensity visual fault indication for the D5A/B LED

- The evaluation platform provides the user two channels (A and B) for analysis which can share the same power supply or be driven independently with different voltages. There is no interaction between the two channels (other than sharing the common GND), and there is no requirement for special power up or power down sequencing. Channel A is populated with the ISL6152 and channel B is populated with the ISL6142, however an additional unit of each product is supplied for analysis. Channel “B” is designed with socketed through-hole components to make modifications and circuit analysis user friendly. The boards are labeled for negative supply operation; GND is the most positive voltage, -VINA and -VINB are the most negative voltages. Note that GND is common for both channels on all three boards. Since most IC signals are referenced to the negative rail, the user may want to reference the voltmeter and oscilloscope GNDs to the negative supply. However, be careful of earth GND connections (on power supplies or oscilloscopes) that don’t match the user’s GND.

- The boards can be used in a positive supply configuration, as long as the user renames (mentally or physically) the signals (GND becomes the positive supply, -VINA/-VINB become the new GND). In this configuration both supplies must be the same voltage.

- The default application circuit is set for a for maximum operating voltage (Over-Voltage threshold) of -56V. A minimum operating voltage of -44.5V is required at power-up (increasing UV threshold) and the device will turn off the FET when the supply drops below approximately -40V.

- The typical load is a -48V to 5V brick regulator which is not included on the load board. However, connector terminals (posts) are provided at the output side of the control board making it easy to connect to a brick regulator or modify the load characteristics if desired.

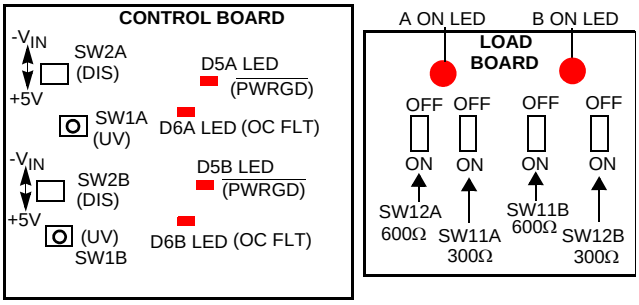


FIGURE 2. LEDs AND SWITCHES

BUS board (Input -48V Power; Fig. 6)

- Multiple large holes for soldering wires, posts, pins, etc. for input power (-48V and GND typical)

- Holes for optional input caps

- Edge connector pins plug into the Control board to simulate/evaluate hot insertions

- Separate GND connector pin that can be modified (trace shortened) and used to simulate last pin making contact. JP1A and JP1B on the Control board must be removed to enable the short pin ground configuration.

CONTROL Board (IC Hot-Plug; Fig. 7)

- Two hot plug channels

- Compare Intersil ISL6142 (L) to ISL6152 (H)

- Easily change application components and evaluate circuit performance with the socketed through hole components of channel B

- Power good (D5A/B) and Over-Current Time-Out (D6A/B) LED “FAULT” indicators. The power good fault LED functions only for the ISL6142. Removing JP3A/3B isolates the $\overline{\text{PWRGD}}$/PWRGD output pin from the fault indicator circuitry for the respective channel. Note that the power good output pin is still connected to the TPPGA/TPPGB test pin on the load board with the jumper removed.

- Push-button Switch (SW1A/B) resets the Over-Current latch by temporarily shorting the UV pin to $-V_{IN}$

- Mini toggle switch SW2 disables the external FET when switched to +5V (with respect to $-V_{IN}$) and resets the Over-Current latch when toggled high to low. Removing JP2A or JP2B allows the user to by-pass the SW2A/B switch and drive the DIS pin externally.

- JP1A and JP1B connect the A3 ground trace from the Bus board (short pin ground) to main ground on the Control board. The jumper should be open if a short pin configuration is desired.

- Footprints for 3 FET outlines; D2PAK, SO-8, SOT-223
- Test points for most IC pins, GND (black), -VINA/B, and $-V_{OUT}$.
- Red test pins (+5VA/B) provided to connect the external +5V supply (referenced to $-V_{IN}$) to the Control board
- Small bread-board area for adding additional circuitry
- Approximate minimum board area highlighted (ch. A)
- Footprints for load capacitors (C5A/B)
- Footprints for RC filter on V_{DD} (channel B only)

- Footprints for DRAIN protection diodes (channel B). Board is shipped with a zero ohm resistor in the D2B place holder.
- Footprint for over voltage clamping suppressor (channel B)
- Option for green LED for Power Good OK (ISL6142 only)
- Alternate 0.020Ω sense resistor included for higher Over-Current threshold setting
- Output load terminals (posts) for modifying load characteristics. TPLD1A and TPLD1B connect to ground, TPLD2A and TPLD2B connect to $-V_{OUT}$ of their respective channels.

LOAD Board (R and C Loads; Fig 8)

- Edge connector pins plug into Control board
- Typical load current is <100mA (limited by power dissipation of the load resistors); Over-Current trip point is ~185mA.
- Two load resistors per channel create approximately 85mA, 160mA or 240mA (resistors in parallel for Over-Current condition) load currents
- Switches to connect the loads in and out
- Multiple holes for soldering wires, pins, posts, for external output load connections (brick regulators are too big and varied to include on the board).
- Holes for optional load capacitors
- Power Good signal ($\overline{PWRGD}$/PWRGD) from each channel brought over through edge connector (TPPGA/TPPGB)
- LED Channel “ON” indication

Operating Instructions

-48V Hook-Up

1. One -48V power supply (0.5A total, 0.25A/channel) and one +5V supply are needed to fully exercise all functions of the device. The user should be sure the +5V supply is referenced to $-V_{IN}$ to avoid damaging the IC. The external +5V supply (PS2) should be connected to the +5VA and +5VB test pins of each channel. The two channels can share the same negative supply ($-V_{IN,}$ PS1) or operate from independent supplies if desired, but they share the same ground plane on each board (bottom). No special power-up or power-down sequencing is required. If only one channel is being tested, the other can be left unconnected. The following instructions are the same for both channels. As shown in Fig. 3, A1 is an optional ammeter to measure current; V1 is a Voltmeter to measure power supply voltage, and V2 is a voltmeter to look at other signals. Note that the voltmeters are referenced to the negative supply rail.

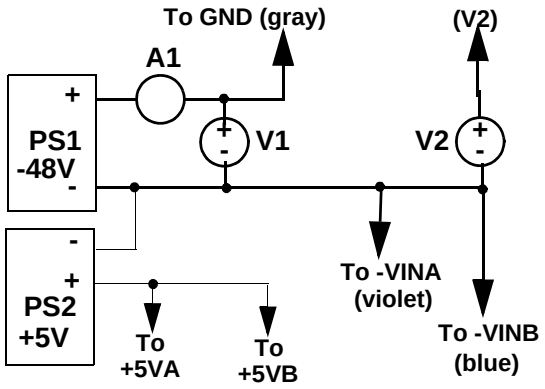


FIGURE 3. SUPPLY AND METER HOOK UP

NOTE: If the user substitutes higher current external loads, the power supply capability would need to be increased accordingly.

2. Begin with all the supplies off.
3. Connect the gray wire to GND (or most positive voltage); connect the -VINA (violet) and -VINB (blue) wire(s) to the most negative supply voltage (typically -48V), connect PS2 to +5VA and +5VB.
4. Plug the 3 boards together; from left to right, should be the BUS, CONTROL, and LOAD boards (those labels should be upright, facing the user). Set the switches on the LOAD board to the “No Load” position (up).
5. Make sure SW2A/SW2B is switched in the “UP” position which ties the DIS pin to $-V_{IN}$ and allows the FET to turn on when the UVLO/UV/OV conditions are satisfied.
6. Check to make sure the +5V supply is referenced to $-V_{IN}$.
7. Turn on the supplies (-48V and +5V). The FETs should turn on, switching the $-V_{IN}$ voltages to $-V_{OUT}$; the A ON and B ON LED(s) on the LOAD board should be on. Power supply current (if monitored) should be about 5mA per channel.

Functional Tests

1. A simple check for UV (Under-Voltage) and OV (Over-Voltage) can be done, with a variable power supply. Increasing the $-V_{IN}$ supply from -48V to -56V will trigger the OV comparator turning off both the external FET and the load board “ON” LED until the voltage is lowered to about -55V. When the OV or UV threshold is exceeded, the power good LED fault indicator (D5B) will light up indicating the power supply is outside its operating range or a fault is present. Note that the $\overline{FAULT}$ pin will not transition low in this case as the fault status pin and the associated LED (D6A/D6B) only flag Over-Current Time-Out events. The UV threshold and hysteresis can be checked by reducing the $-V_{IN}$ voltage to approximately -40V. This triggers the UV comparator which turns off the external FET and lights up LED D5B. The power good Fault LED (D5A) is not compatible with the ISL6152; it will always be on as long as the input power supply is on. That is why the jumper is disconnected.
2. Switch on Loads: At -48V, SW11 by itself will produce ~80mA of current; SW12 by itself should give ~160mA of current. With both loads switched in (parallel) the load current will be in the 240mA range, and exceed the Over-

Current threshold of 185mA (0.05V/0.27ohm = 185 mA). The FET should turn off, the A/B ON LED should go off, the fault LED's D5B and D6B should both turn on. For the ISL6152, D6A will turn on (D5A will always be on). The Over-Current Time-Out is programmable with the C3 capacitor and is set to approximately 600uS. The response is easily monitored with an oscilloscope; connect voltage probes to the GATE and IS_{OUT} pins and initiate the Over-Current event. The GATE pin will be pulled low (~4V) to limit the current to $50mV/R_{SENSE}$ for the programmed time-out period. If the fault persists, the GATE will be pulled to $-V_{IN}$ and the FET will turn off. The user may also want to monitor the load current during this event with a current probe. Load current measurements and the current monitor output (IS_{OUT}) are discussed in greater detail in the Current Monitor section. To return to normal operation, un-switch both load resistors, press and release SW1 or toggle SW2 to +5V and back to $-V_{IN}$. This clears the Over-Current latch and initiates a normal start-up.

3. Disconnect the BUS board from the CONTROL/LOAD boards; now plug it back in; this simulates a hot plug board being inserted into a live connector. The FETs should turn on in a controlled manner, based on the gate timing components. If a load capacitor is added, the user may have to reduce the value of R1 to ensure the Over-Current trip point is not exceeded by the inrush current; or increase the value of C2 to keep the inrush current below the Over-Current threshold. Equation #1 shows the relationship between C2, the load capacitor (C_L) and the inrush current, where I_{PU} is the gate pull-up current (50uA nominal). The Over-Current trip point (I_{OC}) is defined in equation #2. Reference the ISL6142/52 data sheet for more detailed information regarding component selection.

$$I_{inrush} = I_{PU} \times \frac{C_L}{C_2} \quad \text{(EQ. 1)}$$

$$I_{OC} = \frac{50mv}{R_{sense}} \quad \text{(EQ. 2)}$$

4. Disconnect the BUS/CONTROL from the LOAD; now plug it back in; this simulates a load being plugged into a powered motherboard with hot plug protection.

Current Monitoring

The ISL6142/52 has a unique feature that monitors and reports the current flowing through the R1 sense resistor (I_{SENSE}). The IS+ and IS- pins sense the load current. A scaled version of that current is sourced from the IS_{OUT} pin to $-V_{IN}$ through resistor R9, providing a current to voltage conversion. The IS_{OUT} pin will typically be tied to the input of an A to D converter to provide the system real time load/fault current up-dates. The IS_{OUT}/ I_{SENSE} scaling factor is set by the resistor ratio R1/R7. The scale factor for channel A is $0.270\Omega/270\Omega = 0.001$, so IS_{OUT} will source 1uA (through R9 to $-V_{IN}$) for each milli-amp of current flowing through R1. With R9 set to 10KΩ, the voltage on the IS_{OUT} pin will equate to 10mv for each milli-amp of load current. The current scaling factor for channel B (0.000985) is slightly less than that of channel A, as the standard value for the R7/R8 through-hole resistor is 274Ω. To keep the current to voltage scaling factors of the two channels equal, the value of R9B (10.2KΩ) is set slightly higher. With these component values the output voltage to load current ratio is 10.05mV/1.0mA. The current scaling factor is easy to alter on channel B with the through-hole components. If the value of R7 is changed, keep in mind that R8 should match as closely as possible to minimize the error of the current monitor circuit. A match of 1% or better is recommended.

There are several ways to measure the actual load current, as one might be interested in examining the correlation between it and the current monitor output. A voltmeter can be placed across the R1 sense resistor and the current can be calculated (I = V/R; R = 0.27 ohms). However, for a more for accurate measurement and the ability to examine current transients, a current probe connected to an oscilloscope is recommended. First, place all of the load switches in the "No Load" position (up). Connect a wire loop from -VOUTA/B to an external load and then back to GND. There are also a set of connector posts for each channel located next to the FET's which provide the same capability. Each channel has a post that connects to ground (TPLD1A - channel A, TPLD1B - channel B) and a post that connects to -VOUTA/B (TPLD2A - channel A, TPLD2B - channel B). The load resistors can also be used by connecting the wire loop from the output to one of the load resistor terminals closest to the switch. Now the load current will flow through the wire loop, and can be monitored.

Logic Inputs/Outputs

The Logic levels used to drive the DIS input must be referenced to the negative supply rail ($-V_{IN}$). A logic low (<1.5V) will allow the GATE pin to be pulled high and turn on the FET if no fault conditions are present; A logic high (>3.0V) will pull the GATE pin low and turn off the FET. Toggling the pin high and then low will also reset the Over-Current latch if it has been set. The logic levels are applied to the pin with the SW2A/B switch. When the switch is in the up position the DIS pin is connected to $-V_{IN}$ (logic low); in the down position the DIS pin connects to the +5VA/B test pins to produce a logic high). These test pins (red) must be physically connected to the external +5V supply (PS2). Jumpers JP2A/B are provided to allow the user to by-pass the switch and drive the DIS pin externally (TP3 or post of JP2). Also note that a weak internal pull-up device will pull the pin high to an internal +5V rail, creating a logic high if the pin is left open.

The $\overline{FAULT}$ output is an open-drain, pull-down device referenced to V_{EE}. It is pulled active low whenever the Over-Current latch is set. It goes to a high impedance state when the fault latch is reset by toggling the UV or DIS pins. The pull-up resistor (R10) is connected to the +5VA/B test pin

which must be physically connected to the external +5V supply (PS2).

Other Notes

The Over-Voltage trip point (increasing supply) is set to -54V to protect the load resistors; the R4,R5,R6 values can be changed for other loads. A more typical value for OV is around -71V, the high end of the range for a -48V supply application. See the ISL6142 data sheet for more details on how to select the resistors.

There are many test pins that can be used for meter or oscilloscope probes. Discrete components might even be soldered to them if necessary (see the “Board Labels” sections).

Additional or alternative loads can be externally connected to both the Control board and the Load board.

Individual components can be un-soldered and replaced with alternative values, if desired. The through-hole components on channel B make this easier.

Be sure that any added components are properly rated for the application voltage; this is especially true for input or output capacitors. For example, they should be rated for 100V if the full voltage range will be used.

The power good fault LED (D5A/B) is intended for display purposes. The implementation used is not necessarily a satisfactory solution for a production design. Aside from being useful only with the ISL6142, the brightness varies greatly with the supply voltage. If the signal is to be used as a logic output, as well as drive an LED, then the voltage level must also be compatible with the signal it drives. The jumper JP3 disconnects the LED from the pin to separate the functions if desired. The present circuit also clamps the output voltage to approximately 4.5V with a 3V zener diode (D4) which is compatible with most logic levels. Finally, the LED provides a current path between the $\overline{\text{PWRGD}}$ pin back to the V_{EE} pin, when the FET is off; this may not be desirable in the application. Referencing the LED to the DRAIN pin doesn’t work, since under most faults, when the FET turns off, the DRAIN will be floating.

Since the ISL6142 $\overline{\text{PWRGD}}$ output is an open-drain, pull-down device, an LED connected to the positive supply is another option. Since the LED will be on during normal operation, and off during a fault, a green “OK” LED is suggested. See “Optional Components” section for more details.

Board Components (Same for both A and B channels; See Fig. 4 and 7)

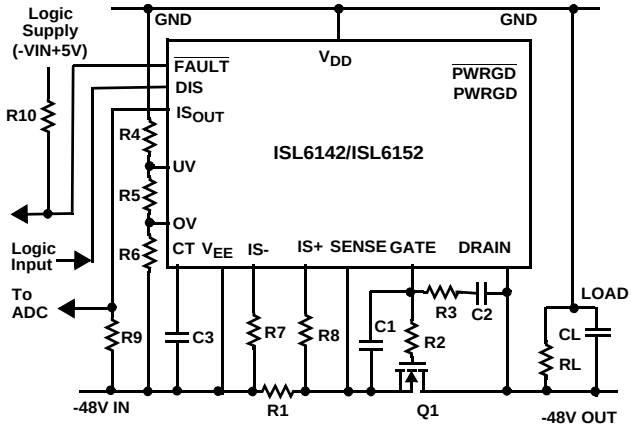


FIGURE 4. TYPICAL APPLICATION

U1 is the ISL6142 (L) or ISL6152 (H) Intersil hot plug controller IC; the only difference between the two part numbers is the polarity of the $\overline{\text{PWRGD}}$/PWRGD output (pin 1). Channel A is populated with the ISL6152; channel B is populated with the ISL6142.

R1 is the Over-Current sense resistor. I_{OC} = 50 mV / R1. If the voltage drop across this resistor exceeds 50mV the time-out circuit will activate and the GATE will be pulled lower (to ~4V) to regulate the current to 50mV/Rsense. If current limiting exceeds the programmed time-out period the fault latch will be set and the FET will be turned off. If the voltage drop across the R1 resistor exceeds 210mV, the hard fault comparator will trip, the FET will be momentarily turned off (timer is reset) and then slowly turned back on for a single retry.

Q1 is the FET that switches the voltage from the input BUS to the LOAD (D2PAK package).

R3, C2, R2, C1 control the inrush current, prevent momentary turn-on during power-up, and keep the gate pin from oscillating. See ISL6142/52 data sheet for more details.

C3 is the capacitor used to program the current limit time-out period. When the Over-Current threshold is exceeded a 20μA (nominal) current source will charge the C3 capacitor from V_{EE} to approximately 8.5V. When the voltage on the CT pin exceeds the 8.5V threshold, the GATE pin will immediately be pulled low with a 70mA pull down device, the Over-Current latch will be set, and the FET will be turned off. If the Over-Current condition goes away before the time-out period expires, the CT pin will be pulled back down to V_{EE}, and normal operation will resume.

R4, R5, R6, are the resistors that divide the input power supply voltage down to the Over-Voltage (OV) and Under-

Voltage (UV) trip points. Reference the ISL6142/52 data sheet for more details.

R7, R8, and R9 are used to sense the load current (R7/R8) and convert the scaled output current (IS_{OUT}) to a voltage (R9). This voltage will typically be the input signal to an A to D converter. Reference the Current Monitor section (page 5) and the ISL6142/52 data sheet for more details.

R10, and D6 create the Over-Current Time-Out fault indicator. R10 is a pull-up resistor for the open-drain $\overline{FAULT}$ output pin which goes active low when the Over-Current latch is set. The output signal is referenced to V_{EE}. The resistor is connected to the +5VA/B (red) test pin which must be externally connected to the +5V supply. The R10A/B resistor is in series with the D6A/B Over-Current fault LED which is tied to the $\overline{FAULT}$ pin.

R12, R13, D4, and D5 create a power good red LED fault indicator for the ISL6142 (L version). R12 sets the LED current; R13 is just a zero ohm placeholder; D5 is the LED, and D4 is a 3V zener diode used to clamp the output high voltage. Note that when the $\overline{PWRGD}$ open-drain pull-down output turns on (Power is Good), the fault LED is off. When the output turns off, the fault LED will turn on. The voltage would rise to a high value, but the zener and the LED will clamp it to approximately 4.5V.

SW1A/SW1B are push button switches used to reset the Over-Current fault latch. When pushed and released the latch is cleared and a normal start-up sequence is initiated.

SW2A/SW2B are mini toggle switches that are used to drive the disable pin (DIS) high or low. When the DIS pin floats or is tied to an external +5V supply (with respect to $-V_{IN}$) the GATE will be pulled low and the FET will be off. When tied to $-V_{IN}$, the GATE will be high and the FET will be on (assuming no fault conditions are present). The purpose of the switch is to demonstrate the functionality of the DIS pin. A typical application could use an N-channel logic FET and additional logic circuitry referenced to the negative supply rail to perform this function. Jumpers JP2A/2B are provided to allow the user to disconnect the switch and drive the DIS pin externally. The switch can also be used to reset the Over-Current latch when toggled high to low. If not used the pin should be tied to the negative supply rail.

Optional Components (Fig. 7)

R11 and C4 (channel B only) make an RC filter for the V_{DD} pin. It is used to isolate some kinds of system supply noise from the IC. For example, it may help filter out glitches that could trigger OV or UV (which shut off the FET) if near their trip points.

D1 (channel B only) is a voltage suppressor, which can help protect the board components from transient voltages that exceed the normal operating range allowed (absolute maximum is 100V).

D2 and D3 (channel B only) may be used to block inductive transients that might pull the drain pin negative with respect to the V_{EE} pin. The ISL6142 (L version) uses one diode (D2), the ISL6152 (H version) uses both diodes. The diodes have a second effect of offsetting the DRAIN trip points for the $\overline{PWRGD}$/PWRGD output. The default board has one of the diodes (D2B) shorted out with zero ohms which should be removed before adding one or two diodes.

Q2 and Q3 are alternate package options for Q1 FETs. Q2 is an 8-pin SOIC, using a standard pinout (S=1, 2, 3, G=4, D=5-8). Q3 is an SOT-223 package. Since all three pins of all three packages are wired in parallel, with no jumpers, it is recommended that only one of the 3 be populated at any given time.

R1_alt is an alternate 0.020Ω sense resistor which can be used to evaluate the device at higher operating currents; if used instead of R1 (un-solder R1, and solder in R1_alt). This resistor will produce an Over-Current trip point of 2.5A (50mV / 0.02Ω). The load resistors supplied with the LOAD board (in parallel) will only produce about 0.25 Amps of output current per channel. To trip the Over-Current threshold of 2.5A, a shorting mechanism or a lower value external load will be necessary. Keep in mind that the power supply must also be rated to handle the higher load current. Also note that if the fault current exceeds the hard fault threshold of 210mV, the GATE will immediately shutdown (10uS typical) and a single retry will follow.

D7 is a green LED that can be used as a $\overline{PWRGD}$ “OK” indicator, instead of a red fault LED. It should only be used with the ISL6142. Resistor R12 sets the LED current; the D7 LED replaces R13, and D4 and D5 are disconnected (remove either one to open circuit).

C5 is a load capacitor that can be placed on the CONTROL board (in addition to the three cap footprints on the LOAD board) to demonstrate inrush current control with a capacitive load for a hot insertion.

BUS Board Labels (See Fig. 11)

- -VINA = J1A, J1B, J1C
- GND = J2A, J2B, J2C
- GND = J3A, J3B, J3C
- -VINB = J4A, J4B, J4C
- C21A = optional input capacitor for -VINA (to GND)
- C21B = optional input capacitor for -VINB (to GND)

Edge Connector Pins (P1)

- Top pins B6, B5, B4 = -VINB
- Top pins B3, B2, B1 = -VINA
- Bottom pins A6 - A1 = GND
- Note that pin A3 is the short pin ground but must be modified (trace shortened) to ensure this pin is the last

one to make contact. It is used in some applications to hold the IC's in reset until all pins are have made good contact. If this is desired, the user must also remove the jumper caps on JP1A and JP1B (Control Board). When this is done the A3 ground trace on the Control board is disconnected from the main ground trace on the control board (see figure 7).

CONTROL Board Labels *(See Fig. 10)*

Edge Connector Jack J1 (input)

- Top pins B6, B5, B4 = -VINB
- Top pins B3, B2, B1 = -VINA
- Bottom pins A6, A5, A4, A2, A1 = GND
- Bottom pin A3 = SHORT GND trace - simulates last pin to make contact; connected to the UV/OV resistor divider on both channels)
- JP1A and JP1B tie the short pin ground to main ground effectively eliminating the shorter pin if it has been modified. If the SHORT GND function is desired simply disconnect the jumpers and the UV/OV resistor divider will only be connected to the short pin ground trace (A3).

Edge Connector Jack J2 (output)

- Top pins B6, B5, B4 = -VOUTB
- Top pins B3, B2, B1 = -VOUTA
- Bottom pins A5, A4, A3, A2, = GND
- Bottom pins A1 = PWRGDA; A6 = $\overline{\text{PWRGD}}$B; These signals are brought over to the LOAD board (TPPGA, TPPGB) in the event the user needs them (for example, to enable a brick regulator).

Test Pins

- -VIN1A, -VIN2A, -VIN3A (channel A - white)
- -VIN1B, -VIN2B, -VIN3B (channel B - white)
- GND1 - GND4 (channel A and B share ground - black)
- +5VA, +5VB (red) must be tied to an external +5V supply (with respect to $-V_{IN}$)
- TP1A -TP5A, TP7A, TP8A, TP10A -TP14A; each pin has its own test point with the exception of pins 6 and 9)
- TP1B -TP5B, TP7B, TP8B, TP10B - TP14B, each pin has its own test point with the exception of pins 6 and 9)
- -VOUTA, -VOUTB

Load Terminals

- TPLD1A, TPLD1B (connect to ground)
- TPLD2A (-VOUTA), TPLD2B (-VOUTB)

Switches

- SW1A/SW1B is a push button switch used to clear the Over-Current latch by momentary shorting the UV pin to the negative supply rail.
- SW2A/SW2B are mini toggle switches used to drive the DIS pin low or high to control the GATE drive. Also used to reset the Over-Current latch by toggling high to low.

Jumpers

- JP1A/JP1B connect the short pin ground trace (A3) on the Control board to main ground (A1, A2, A4-A5). Both jumpers should be removed if the user wishes to simulate last pin contact. In this case only the A3 trace will connect to R4. Also note that the A3 trace on the Bus board must be shortened by the user.
- JP2A/JP2B connects the $\overline{\text{DIS}}$ pin to the SW2A/SW2B mini toggle switch. By removing the jumper cap, the user can drive the disable pin externally with a signal generator or external logic referenced to $-V_{IN}$.
- JP3A/JP3B connects the $\overline{\text{PWRGD}}$ /PWRGD output (pin 1) to the red fault LED indicator (D5A/B). This jumper should be removed for the ISL6152 (H version) because the LED circuit is not valid; the LED would remain on for either output state. Also the jumper should be removed if the LED circuit interferes with the logic levels needed externally (such as for a brick regulator). The present board clamps the output to ~4.5V when the LED is on. Note that this circuit may not be the most efficient or cost-effective; it is just meant to be functional for the Eval board.

LEDs

- D5A/D5B are red power good "FAULT" indicators. The LED comes on if the $\overline{\text{PWRGD}}$ pin on the ISL6142 goes high; it represents some kind of fault, usually a shorted output or an Over-Current shutdown. The LED will also turn on if the FET is turned off due to a UV or OV fault. It will turn back off when the supply is back within tolerance.
- D6A/D6B are Over-Current Time-Out "FAULT" indicators. They turn on only when the Over-Current fault latch is set due to a current limit time-out. The LED will turn off when SW1A/B is pushed or SW2A/B is toggled high to low

LOAD Board Labels *(See Fig. 9)*

CAUTION HOT

The load resistors are mounted on the bottom of the LOAD board, but the heat can be felt through the top of the board. Be careful how you handle the board, especially while gripping it for plugging or unplugging.

Edge Connector Pins (P2)

- Top pins B6, B5, B4 = -VOUTB
- Top pins B3, B2, B1 = -VOUTA
- Bottom pins A5, A4, A3, A2 = GND
- Bottom pins A1 = PWRGDA; A6 = $\overline{\text{PWRGD}}$B

Test Pins

- TPPGA (pin A1); PWRGDA
- TPPGB (pin A6); $\overline{\text{PWRGD}}$B
- TPG (pin A5 - A2); GND
- TPA (also J5A, J5B, J5C); -VOUTA
- TPB (also J6A, J6B, J6C); -VOUTB
- J7A, J7B, J7C, J8A, J8B, J8C; GND

Optional Capacitors

- C11A, C12A, C13A; for -VOUTA
- C11B, C12B, C13B; for -VOUTB

Switches *(note the Load and No Load positions)*

- SW11A switches load R11A (330Ω) in or out (-VOUTA)
- SW12A switches load R12A (620Ω) in or out (-VOUTA)
- Both Switches together should create an Over-Current shutdown for Channel A (with R1 = 0.27 ohms)
- SW11B switches load R11B (330Ω) in or out (-VOUTB)
- SW12B switches load R12B (620Ω) in or out (-VOUTB)
- Both Switches together should create an Over-Current shutdown for Channel B (with R1 = 0.27 ohms)

LEDs

- D11A is on when -VOUTA is switched on (through the Q1A FET). Note it is independent of whether either of the load resistors are connected.
- Same as above for Channel B.

ISL6142/52 EVAL BOARDS (BUS INPUT, CONTROL, LOAD OUTPUT)

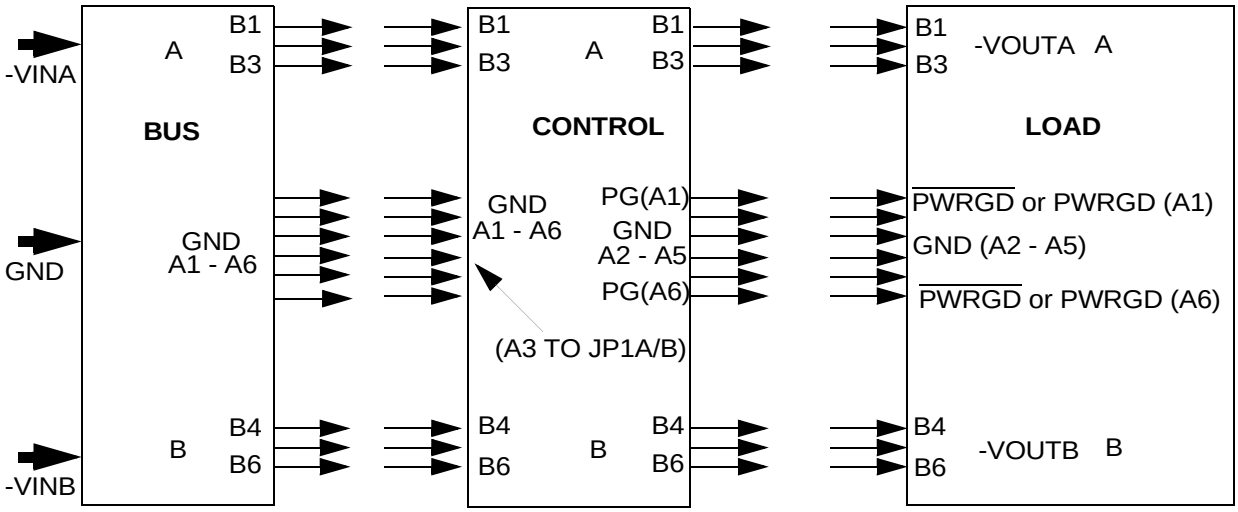


FIGURE 5. THREE BOARD SET

ISL6142/52 EVAL Boards BUS (Input)

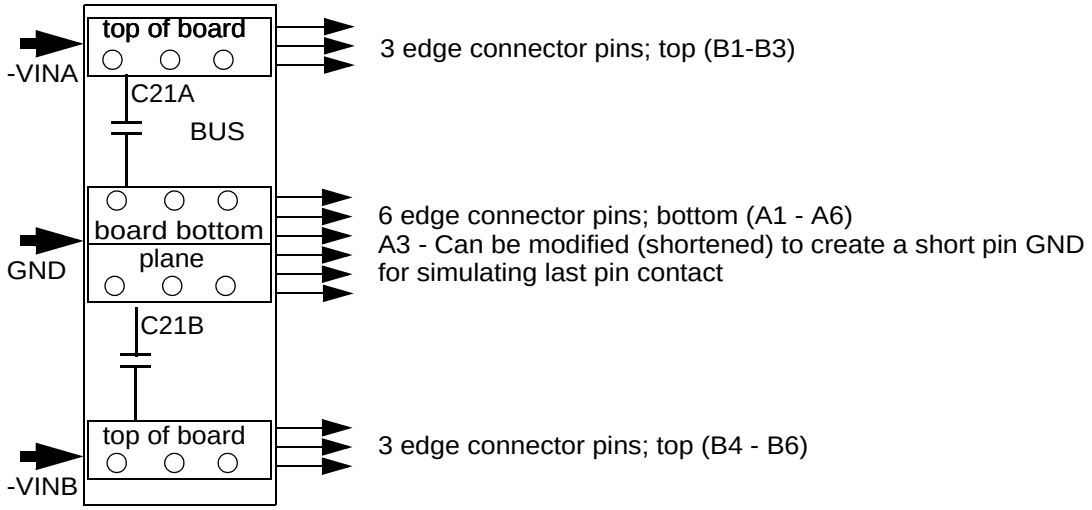


FIGURE 6. BUS BOARD SCHEMATIC

ISL6142/ISL6152 Customer Evaluation Board

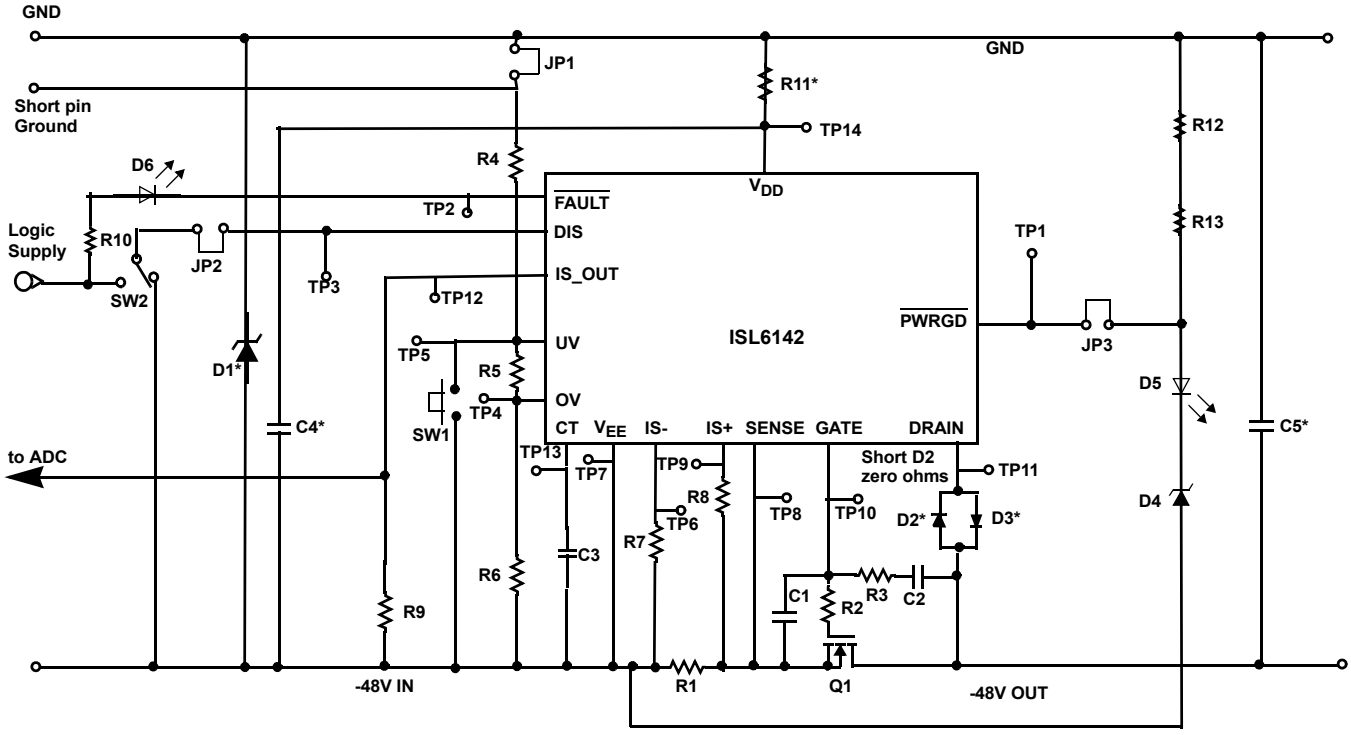


FIGURE 7. CONTROL BOARD SCHEMATIC

ISL6142/52 EVAL boards LOAD (Output)

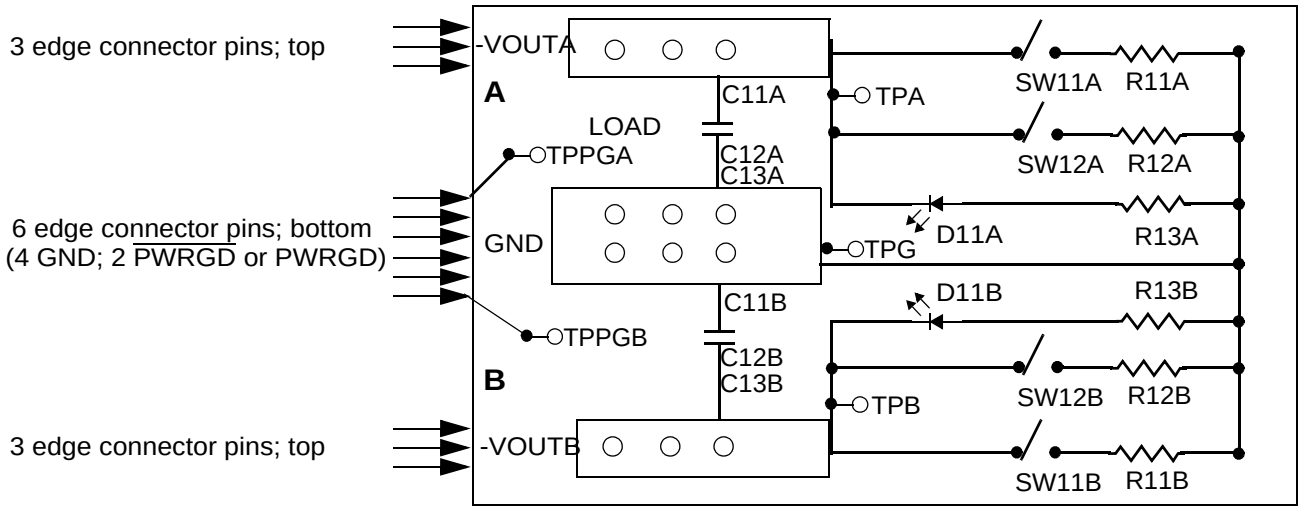


FIGURE 8. LOAD BOARD SCHEMATIC

Bill Of Material

TABLE 1. BILL OF MATERIAL

Component	Name	Size, value, Wattage	Description
	CONTROL BOARD BOM		
U1 A/B	ISL6152 (A); ISL6142 (B)	14-SOIC	
Q1 A/B	IRF530 or equivalent	SMD-220 (D2PAK)	
Q2 A/B	Optional FET	8-SOIC	DNP
Q3 A/B	Optional FET	SOT-223	DNP
R1 A/B	Current Sense Resistor	2512, 0.27Ω, 5%, 1W	Current Limiting Sense Resistor (185mA)
R1_alt A/B	Current Sense Resistor (alternate)	2512, 20Ω, 1%, 1W	Current Limiting Sense Resistor (2.5A)
R2 A/B	Gate Resistor	0805, 10Ω, 5%	
R3 A/B	Power-up Resistor	0805, 18KΩ, 5%, 0.1W / Axial, 18.2KΩ	
R4 A/B	UV/OV Resistor Divider	0805, 562KΩ, 1%, 0.1W / Axial, 562KΩ	UV/OV Programming Resistor
R5 A/B	UV/OV Resistor Divider	0805, 3.3KΩ, 1%, 0.1W / Axial, 3.3KΩ	UV/OV Programming Resistor
R6 A/B	UV/OV Resistor Divider	0805,13.0KΩ, 1%, 0.1W / Axial, 13.0KΩ	UV/OV Programming Resistor
R7A/B	IS- Sensing Resistor	0805, 270Ω, 1%, 0.1W / Axial, 274Ω	Current Sense Output Scaling Resistor
R8A/B	IS+ Sensing Resistor	0805, 270Ω, 1%, 0.1W / Axial, 274Ω	Current Sense Output Scaling Resistor
R9 A/B	IS_{OUT} Resistor	0805, 10KΩ, 1%, 0.1W / Axial, 10.2KΩ	Current Monitor Output Resistor (provides current to voltage conversion and scaling)
R10 A/B	$\overline{\text{Fault}}$ Pull-up Resistor	0805, 3.0KΩ, 10%, 0.1W	$\overline{\text{Fault}}$ Pull-up and LED Bias Resistor
R11B*	Placeholder, RC Filter for V_{DD})	Axial, 0.0Ω	Optional RC Filter (with C4)
R12A/B	LED Bias Resistor	0805, 39KΩ, 5%, 0.25W	
R13A/B	Placeholder	0805, 0.0Ω	Optional Green “OK” LED
C1 A/B	Power-up Capacitor	0805, 150nF, 25V	
C2 A/B	Feedback Capacitor	0805, 3.3nF, 100V / Axial, 3.3nF	
C3 A/B	OC Time-Out Programming Capacitor	0603, 1500pF / Radial, 1500pF, 25V, 10%	Over Current Time-Out programming Capacitor
C4B*	Optional RC Filter for V_{DD}	0805, 0.1uF,100V	
C5* A/B	Load Capacitor	Electrolytic, Radial, 100V	DNP (Through-hole)
D1 A/B*	SMAT70A	SMA	DNP, Voltage Suppressor
D2,D3 A/B*	1N4148	SOD-123; 75V	DNP, Blocking diode
D4 A/B	3V Zener Diode	S-mini 2P	Bias Diode for Power Good Fault - Inactive High
D5 A/B	Red LED	0805	Power Good Fault Indicator
D6 A/B	Red LED	0805	Over-Current Time-Out Fault Indicator
SW1 A/B	UV Reset Push Button;		Normally Open
SW2 A/B	Mini Toggle Switch for DIS Input Logic Control	SMT, SPDT	
JP1A/B	Two Pin Jumper; Shorting Shunt		Enables Short Pin GND Configuration (when open)
JP2A/B	Two Pin Jumper; Shorting Shunt		Isolates DIS Pin Prom SW2A/B (when open)
JP3A/B	Two Pin Jumper; Shorting Shunt		Isolate $\overline{\text{PWRGD}}$/PWRGD Fault LED Circuit (when open)

TABLE 1. BILL OF MATERIAL (Continued)

Component	Name	Size, value, Wattage	Description
	BUS BOARD BOM		
C21 A/B	Optional Input Capacitor	electrolytic	DNP (Through-hole)
	LOAD BOARD BOM		
R11 A/B	Load Resistor	620Ω, 5%, 5W, Axial	Through-hole
R12 A/B	Over-Load Resistor	330Ω, 5%, 10W, Axial	Through-hole;
R13 A/B	LED Current Resistor	39KΩ, 5%, 1/4W	Through-hole;
D11 A/B	Red LED	T1-3/4	Through-hole;
SW11 A/B SW12 A/B	Load Slide Switch		Through-hole;
C11 A/B C12 A/B C13 A/B	Optional Load Capacitors	Electrolytic	DNP, (Through-hole)
	Note: Surface Mount Resistors are 1/10W unless otherwise noted		
	Note: DNP = Do Not Populate		

Component Placement and Labels

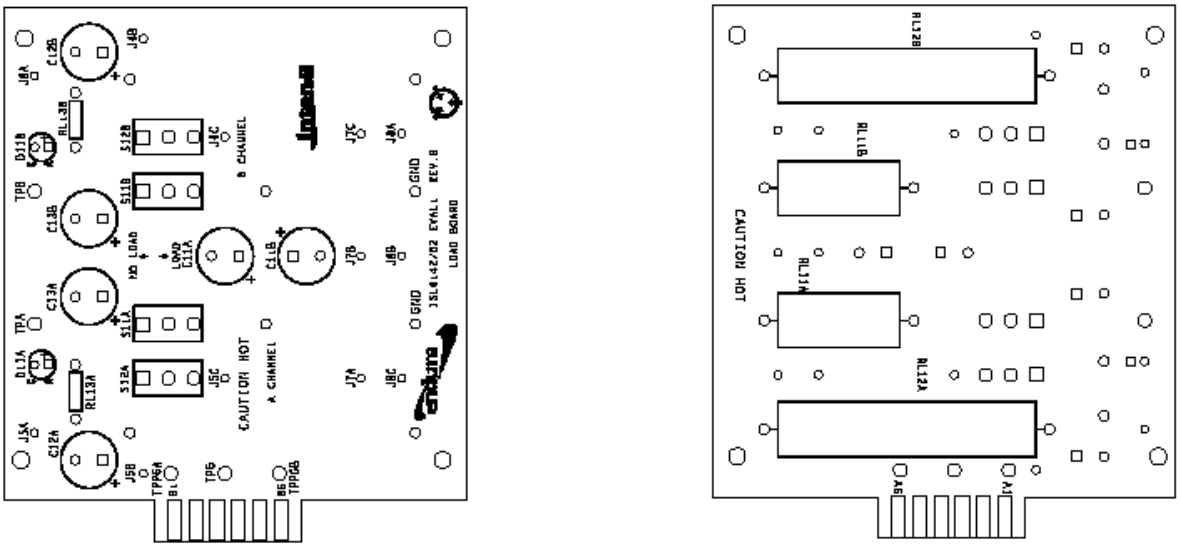


FIGURE 9. LOAD BOARD

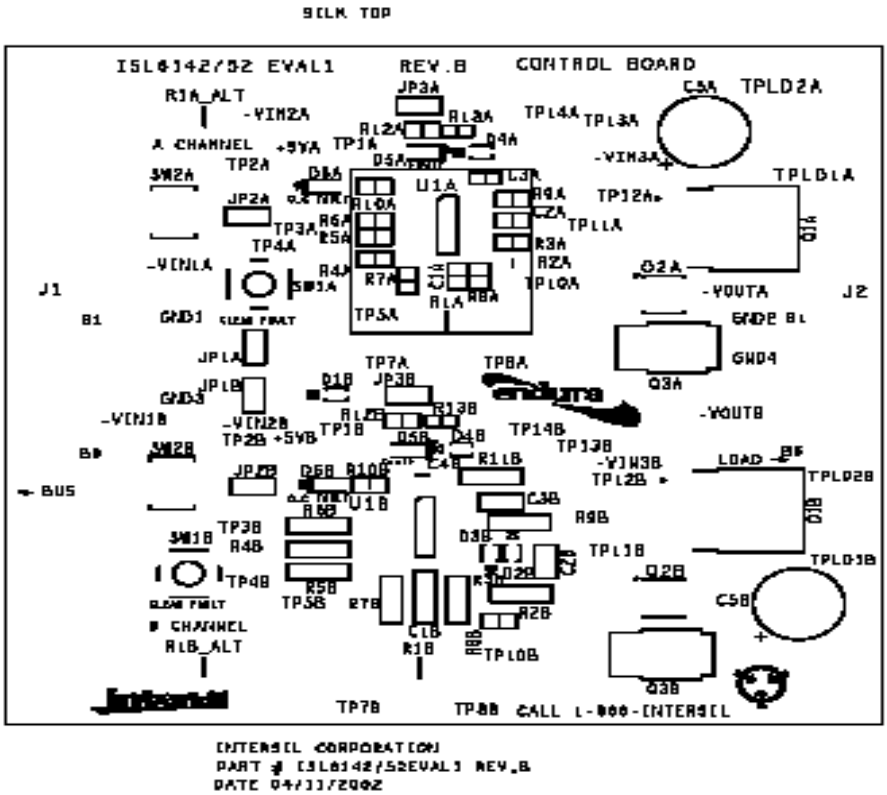


FIGURE 10. CONTROL BOARD

Component Placement and Labels

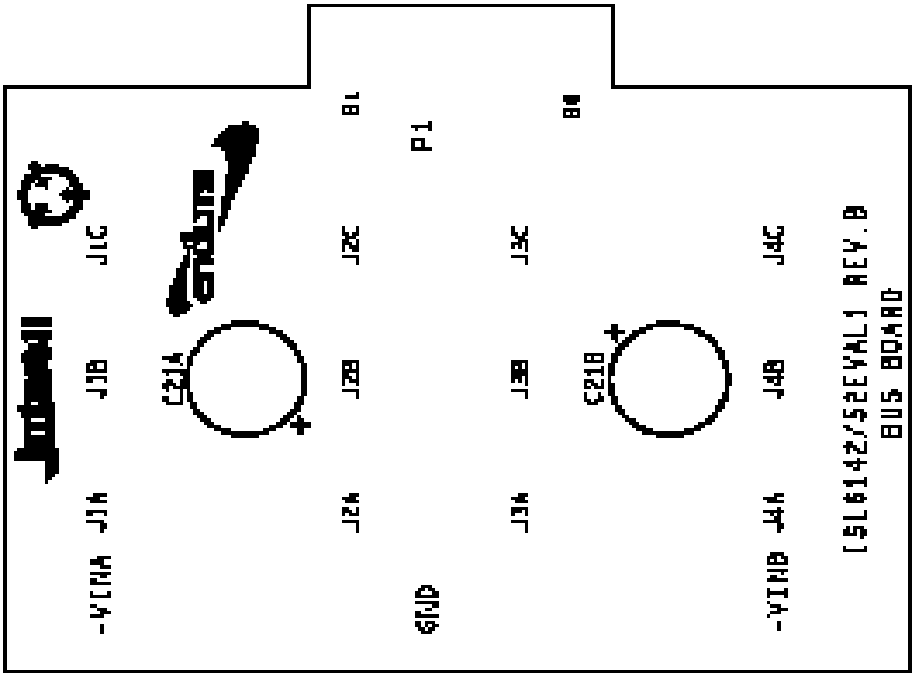


FIGURE 11. BUS BOARD